10

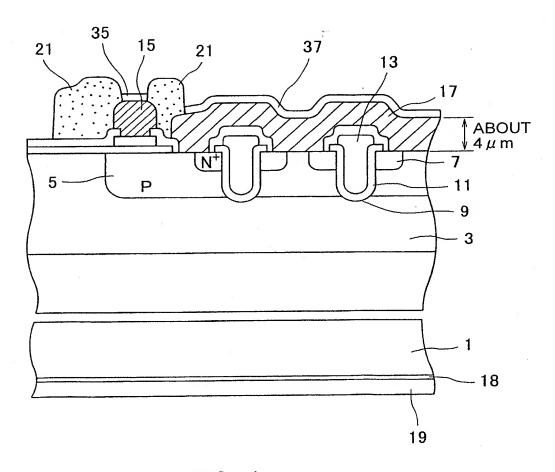
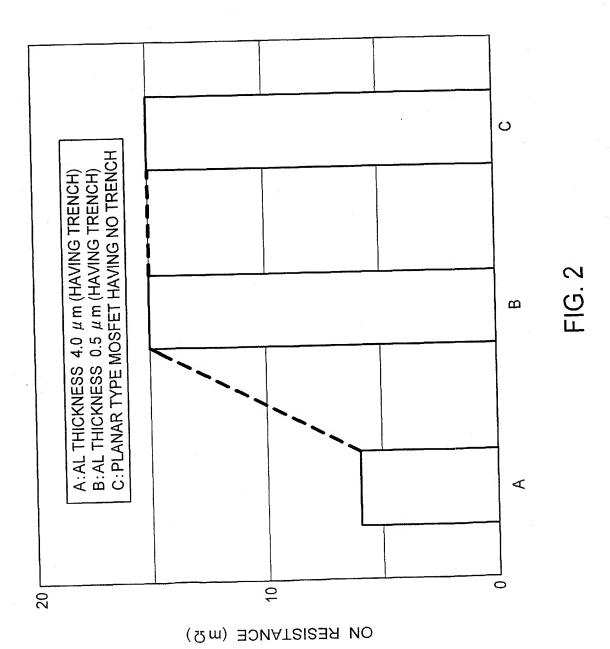


FIG. 1

The state of the s



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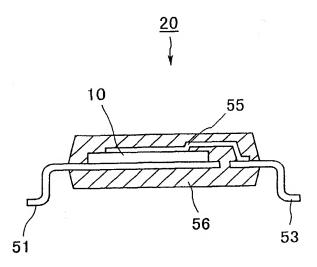


FIG. 3A

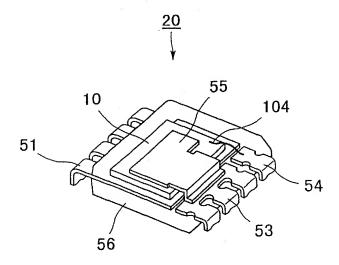
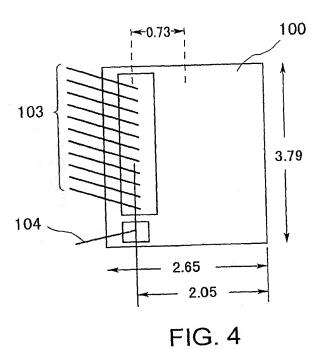


FIG. 3B



the state of the s

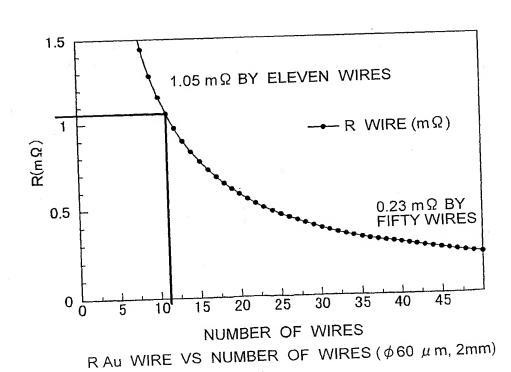
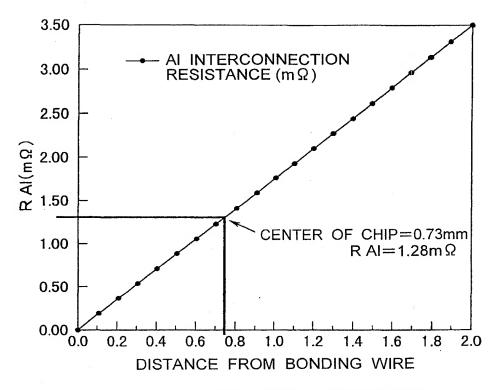


FIG. 5



AI INTERCONNECTION RESISTANCE ON SURFACE OF CHIP

FIG. 6

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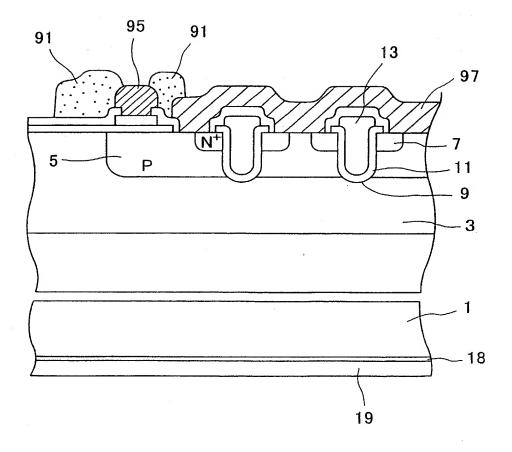


FIG. 7

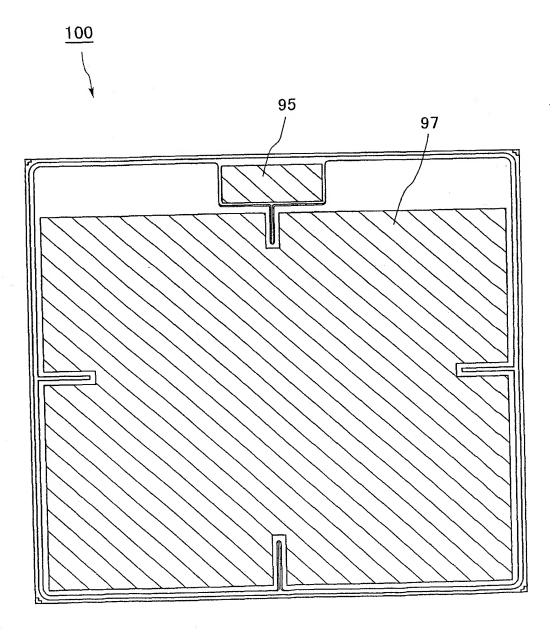


FIG. 8

The state of the s



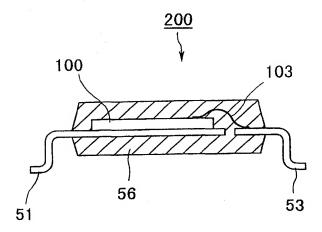


FIG. 9A

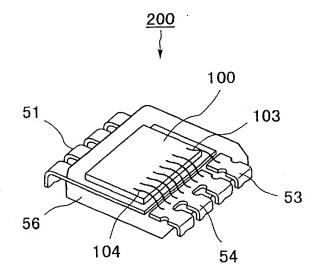


FIG. 9B

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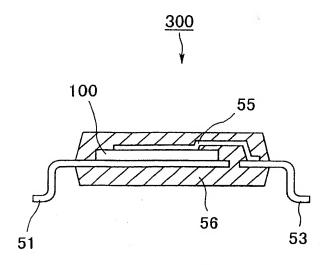


FIG. 10A

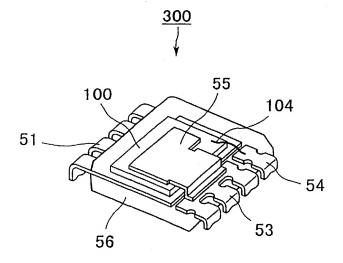


FIG. 10B